ABSTRACT OF THE DISCLOSURE

A video processor comprises a bit rate converter for converting an M-bit input video signal to an N-bit output video signal by retaining gray levels of the M-bit input video signal (where, N is smaller than M). A number of N-bit input gray levels are mapped in a gamma correction memory to a number of output gray levels. The output gray levels are distributed on a non-linear curve complementary to a non-linear curve on which gray levels of a display device are distributed. The memory delivers one of the output gray levels when the N-bit output video signal of the bit rate converter corresponds to one of the N-bit input gray levels. In one embodiment, the bit rate converter truncates lower significant bits of the M-bit video signal, represents the truncated bits by a different number of binary-1's, and distributes the binary-1's over a varying number of subsequent frames depending on the value of the truncated bits.